multi-dimensional programmable cell architecture; and

a [first] plurality of individual lines positioned within the processing unit, the [first] plurality of individual lines being bundled;

wherein the [first] plurality of individual lines provide [a means to communicate] communication between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device.

20. (Amended) [The] A bus system [of claim 19], [further] comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a first plurality of individual lines positioned within the processing unit, the first plurality of individual lines being bundled; and

at least one ~~interface~~ unit coupled to the plurality of individual lines, the at least one interface unit combining the first plurality of individual lines to form the bus system, the first plurality of individual lines providing communication, via the at least one interface unit, between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device.

23. (Amended) The bus system of claim 20, further comprising:

an address generator in communication with the processing unit, the address generator [for] generating an address for selecting a unit coupled to the bus system.

~~28~~ 8. (Amended) [The] A bus system [of claim 27], comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a first plurality of individual lines positioned within the processing unit, the first plurality of individual lines being bundled, the first plurality of individual lines providing communication between the

processing unit and at least one of: i) an additional processing unit, ii) a memory device and iii) a peripheral device;

at least one interface unit coupled to the plurality of individual lines, the at least one interface unit combining the plurality of individual lines to form the bus system;

B3 end

a bus master unit coupled to the plurality of lines and controlling the bus system; and

a plurality of slave units in communication with the bus master unit;

wherein control of the bus system is transferred dynamically from the bus master unit to another unit coupled to the bus system.

---

sub C4

30. (Amended) The bus system of claim 20, further comprising:

a register in communication with the at least one interface unit, the register indicating whether data is stored in the at least one interface unit.

11

~~31~~. (Amended) [The] A bus system [of claim 20], comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a first plurality of individual lines positioned within the processing unit, the first plurality of individual lines being bundled, the first plurality of individual lines providing communication between the processing unit and at least one of: i) an additional processing unit, ii) a memory device and iii) a peripheral device; and

B4

at least one interface unit coupled to the plurality of individual lines, the at least one interface unit combining the first plurality of individual lines to form the bus system, [wherein] the at least one interface unit being [is] at least one of integral with the processing unit and formed by a configuration of [at] a plurality of logic cells, each of the plurality of logic cells implementing simple logical functions according to a logic cell configuration.

31

12 ~~32~~. (Amended) [The] A bus system [of claim 20], comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a first plurality of individual lines positioned within the processing unit, the first plurality of individual lines being bundled, the first plurality of individual lines providing communication between the processing unit and at least one of: i) an additional processing unit, ii) a memory device and iii) a peripheral device; and

at least one interface unit coupled to the plurality of individual lines, the at least one interface unit combining the first plurality of individual lines to form the bus system, [wherein] the [plurality of interfaces are] at least one interface unit being configured by at least one of a primary logic unit and the processing unit.

B4 end 13 ~~33~~. (Amended) The bus system of claim 12 ~~32~~, wherein the [primarily] primary logic unit is at least partially integrated with the processing unit.

Sub C5 34. (Amended) The bus system of claim 20, further comprising:

at least one connection to at least one of a [DFP] data flow processor (DFP), [an FPGA] a field programmable gate array (FPGA), and a [DPGA] dynamically programmable gate array (DPGA).

Please add the following new claims:

Sub C6 35. (New) The bus system according to claim 19, wherein the memory device is external to the processing unit.

B5 36. (New) The bus system according to claim 20, wherein the memory device is external to the processing unit.

37. (New) The bus system according to claim 19, wherein the processing unit includes a plurality of re-programmable, dynamically reconfigurable cells.

37